AMENDMENT TO THE SPECIFICATION

Please substitute the title to read as follows:

-- SIGNAL PROCESSING DEVICE AND SIGNAL PROCESSING METHOD INCLUDING RE-SAMPLING AND A DELAY UNIT --

Please substitute the paragraphs beginning at page 2, line 7 and ending at page 3, line 12 to read as follows:

-- The present invention provides a signal processing device and method which fulfill this requirement. Since the signal processing device and the signal processing method of the present invention perform up-sampling of the multi-channel audio signals which are read out from the recording medium. The device and method compensate the time delay of the audio data according to this up-sampling. Therefore, it becomes possible easily to adjust the phase when reproducing the two audio signals by adapting the processing characteristics of the up-sampling filter to the processing unit for data, and also by adapting the processing unit for decoding of the data to the processing

characteristics of the up-sampling filter. ~~And, moreover~~ Moreover, the present invention provides a disk player which implements this signal processing method.

In order to do this, the signal processing device of the present invention includes a decoder, a filter and a delay unit. The decoder decodes a data stream which includes first and second audio data sampled at different sampling frequencies fs1 and fs2, with fs1<fs2. ~~And the~~ The decoder inputs encoded data and separates them as the first and second audio data. Among the first and second audio data which are outputted from the decoder, the filter performs re-sampling of the first audio data at the same sampling frequency fs2 as that of the second audio data, and suppresses~~,~~ aliasing distortion due to re-sampling. ~~And, among~~ Among the first and second audio data which are outputted from the decoder, a delay unit delays the second audio data by just the amount of processing period due to the filter, and outputs it as a second audio data. --

Please substitute the paragraph beginning at page 4, line 18 and ending at page 5, line 3 to read as follows:

-- The inventors of the present application have pursued the study and development of audio reproducing devices for many years. ~~And the~~ The inventors are currently performing investigation and development, within the limitations of the specifications for the values of recording capacity and output bit rate of a video signal and an audio signal which are recorded upon an optical disk, to make it more possible both to enhance the sound quality of the audio signal and also to increase the number of channels thereof. --

Please substitute the paragraph beginning at page 5, line 14 and ending at page 6, line 4 to read as follows:

-- Fig. 1 is a block diagram showing the structure of an encoding device, which samples two audio signal streams at different sampling frequencies for recording them upon an optical disk described above. This encoding device converts the two audio signals into a first audio data and a second audio data, and encodes these two signals of audio data as a single data stream. Analog audio signals S1 and S2 are inputted to this encoding device via terminals 1 and 2. A sampling circuit 3

inputs the audio signal S1, performs sampling at a sampling frequency fs1 of 48 kHz or 44.1 kHz, and converts it to the first audio data. ~~And a~~ A sampling circuit 4 inputs the audio signal S2 of the second stream, performs sampling at a sampling frequency fs2(=2×fs1), i.e. 96 kHz or 88.2 kHz, and converts it to the second audio data. --

Please substitute the paragraphs beginning at page 6, line 17 and ending at page 8, line 13 to read as follows:

-- A prototype signal processing device has been manufactured which separates a data stream of this type which has been read out from an optical disk into its several constituent data streams. A block diagram of this signal processing device is shown in Fig. 2. The output data stream from the above described recording and reproducing device or transmission device is inputted to a terminal 7 of this signal processing device, and a decoding circuit 8 divides the encoded data stream D3 one block at a time into the original audio data D1 and D2 of two different types. ~~And the~~ The decoding circuit 8 outputs the first audio data D1 to a buffer 9, and outputs the second audio data D2 to a

buffer 10. ~~And an~~ An up-sampling circuit 11 inputs the first audio data D1 at a sampling frequency of 48 kHz or 44.1 kHz, and performs up-sampling thereof at approximately twice as high as the frequency, so as to convert it to an audio data at a sampling frequency of 96 kHz or 88.2 kHz. A D/A converter 12 converts the up-sampled audio data into an analog audio signal. ~~And a~~ A D/A converter 13 converts the output data from the buffer 10 into an analog audio signal. These analog audio signals are output to the outside via respective output terminals 14 and 15.

Fig. 3 shows the audio data which have been sampled by the sampling circuits 3 and 4. D11, D12, D13 ... are data elements of the audio data which has been sampled by the sampling circuit 3. ~~And~~ D211, D212, D221, D222, D231, D232 ... are data elements of the audio data which has been sampled by the sampling circuit 4. In this manner, the first sampling frequency for the first audio data is two times higher than that of the second sampling frequency. In other words, the data which has been sampled by the sampling circuit 3 corresponds to about half the quantity of data which has been sampled by the sampling circuit 4.

Fig. 4 shows the data stream D3 which has been encoded by the encoding circuit 5. The encoding is arranged so that the

reproducing times in analog form of the data elements which have been sampled should be the same. For example, the arrangement may have two data elements of D2j (j=11, 12, 21, 22, ... 401, 402) following after one data element of D1i (i=1, 2, ... 40), so that 40 samples of data from the sampling circuit 3 and 80 samples of data from the sampling circuit 4 constitute one block. ~~And the~~ The encoding circuit 5 appends to each block header data ("Header"), which records the sampling frequency for its data and the like. --

Please substitute the paragraphs beginning at page 10, line 7 and ending at page 11, line 20 to read as follows:

-- The decoding circuit 16 is a circuit which inputs via a terminal 7 a data stream D3 in which the first and second audio data have been encoded and combined by an encoding circuit like the encoding circuit 5 of Fig. 1, and which, by referring to the header data, separates said data stream D3 into a first audio data D1 and a second audio data D2 and decodes them, thus returning to respective audio data at sampling frequencies fs1 and fs2. The buffer 9 is a device for temporarily storing the

first audio data D1. ~~And the~~ The buffer 10 is a device for temporarily storing the second audio data D2.

The up-sampling circuit 17 is a filter which, among the plurality of streams of audio data which are outputted from the decoding circuit 16, performs re-sampling of the first stream of audio data D1 at the high sampling frequency fs2 which is the same as that of the second audio data D2, and which outputs a first stream of audio data in which aliasing distortion generated by this re-sampling has been suppressed. This up-sampling circuit 17, as shown in Fig. 6, comprises a re-sampling circuit 17a and an FIR filter 17b. The re-sampling circuit 17a is so constituted that, when for example it inputs the values D11, D12, D13 ..... in the first audio data D1, it inserts a value "zero" in between each data element and the next, so as to double the number of output data items. ~~And the~~ The FIR filter 17b is a low pass filter which suppresses the aliasing distortion generated by this re-sampling.

The delay buffer 18 is so constituted that, among the plurality of streams of audio data which are outputted from the decoding circuit 16, it introduces a delay period which is just the processing period of the up-sampling circuit 17 into the

second stream of audio data D2 whose sampling frequency is fs2, then outputting it as the second audio data D2. ~~And the~~ The D/A converter 12 is a circuit which converts the output data from the up-sampling circuit 17 into analog form, then outputting it via the output terminal 14 to the outside. Moreover, the D/A converter 13 is a circuit which converts the output data from the delay buffer 18 into analog form, then outputting it via the output terminal 15 to the outside. --

Please substitute the paragraph beginning at page 17, line 16 and ending at page 18, line 16 to read as follows:

-- It should be understood that it is possible to include the above described type of signal processing device function or signal processing method in an optical disk reproducing device. Furthermore, the signal processing device function or signal processing method may be used in the form of a software program or of an application program on a personal computer. In such a case, the function of the decoding circuit 16 or 19 is implemented by a decoding step in which the encoded data stream is inputted, and the audio data streams are respectively

recovered at their original sampling frequencies. Furthermore, the function of the up-sampling circuit 17 performs as a filtering step which includes a re-sampling step and an aliasing distortion suppression step. In the re-sampling step, among the first and second audio data streams outputted from the decoding step, re-sampling is performed upon the audio data stream which has the low sampling frequency of fs1 at the sampling frequency fs2. In the aliasing distortion suppression step, aliasing distortion is suppressed. ~~And the~~ The function of the delay buffer is implemented by a delay processing step in which, among the first and second audio data streams outputted from the decoding step, the audio data stream which has the high sampling frequency is delayed by the delay period equal to the processing period due to the filtering step, and the resulting audio data is outputted. --